REMARKS

Claims 1-12 are pending in this application, of which claims 8-12 are withdrawn from consideration. Claims 1 and 6 are amended with the present Response. Applicant respectfully submits that no new matter has been added.

Claims 1-6 stand rejected under 35 U.S.C. § 103 as obvious over **Seshan et al.** (U.S. Patent No. 6,163,065) in view of applicant's "Admitted Prior Art" (APA). Applicant respectfully traverses this rejection.

Independent claim 1 recites

> "a conductive wall ... in *each* of said first and second interlayer insulation films ..., said conductive wall changing a direction thereof repeatedly and alternately in one of a triangular wave pattern and a rectangular wave pattern ..."

(*emphasis added*). Applicants acknowledges that **Seshan et al.**, in Figure 5, disclose integrated circuit 500 with a plurality of conductive walls (metal layers M1-M5).

However, **Seshan et al.** only teach the alternating wave patterns in one conductive wall, metal layer M5, which forms guard ring 504. Column 4, in lines 32-34, explains that the alternating wave patterns prevent breaking, sheering, and delamination of the guard ring. Because the reference discloses the alternating wave pattern only in the top metal layer, it suggests that the single alternating wave pattern in only the top metal layer is adequate to prevent the mechanical

deterioration. (**Seshan et al.** do not address problem associated with chemical mechanical polishing.) Applicant finds no teaching or suggestion in the reference to add to the complexity of the manufacturing process by forming the alternating wave patterns also in metal layers M1-M4.

Applicant acknowledges that the applicant's Admitted Prior Art (APA) is applied as supposedly suggesting the modification of the **Seshan et al.** semiconductor device to render claim 1 obvious. However, neither Figure 2 (referenced in the Office Action) nor the rest of the APA discloses that it was known to form alternating wave patterns in *each* conductive wall of the guard ring pattern. Therefore, the APA cannot suggest modifying the semiconductor device of **Seshan et al.** to render claim 1 obvious. Therefore, the obviousness rejection should be withdrawn, and claim 1 should be allowed.

Claims 2-6 depend from claim 1. Therefore, because the obviousness rejection of claim 1 should be withdrawn, the obviousness rejection of claims 2-6 should also be withdrawn.

Claim 7 stands rejected under 35 U.S.C. § 103 as obvious over **Seshan et al.** and APA, and further in view of Japanese Patent 10-335456. Applicant respectfully traverses this rejection. Claim 7 depends ultimately from claim 1, and the obviousness rejection of claim 1 should be withdrawn, as explained above. Therefore, the obviousness rejection of claim 7 should also be withdrawn for at least the reason of its dependency from claim 1.

Applicant acknowledges that an additional reference, Japanese publication 10-335456, is applied, but the teaching relied upon in that reference does not cure the above-noted deficiency in either **Seshan et al.** or APA to render base claim 1 obvious. Therefore, the obviousness rejection of claim 7 should be withdrawn.

With the present amendment, applicant amends claim 6 as shown above to correct a minor error.

In view of the amendments and remarks above, applicant submits that the entire application is in condition for allowance. Accordingly, a Notice of Allowability is hereby requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**"

REQUEST FOR PERSONAL INTERVIEW

With the present Response and Request for Continued Examination (RCE) filed concurrently, applicant now requests that, if for any reason it is felt that this application is not now in condition for allowance, the Examiner grant a personal interview with the undersigned representative. Please contact applicant's attorney at the telephone number indicated below before issuing an additional rejection, if an additional rejection is ultimately deemed appropriate by the Examiner.

In the event that any fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with Markings to Show Changes Made

Q:\FLOATERS\JLF\00\000294\preliminary amendment

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims 1 and 6 as follows:

1. (Twice Amended) A semiconductor device, comprising:

a substrate; and

a multilayer interconnection structure formed on said substrate,

said multilayer interconnection structure including: at least first and second interlayer insulation films provided on said substrate; and a guard ring pattern embedded in each of said first and second interlayer insulation films, said guard ring pattern extending along a periphery of said substrate, said multilayer interconnection structure being planarized by using a CMP process,

wherein said guard ring pattern changes a direction thereof repeatedly and alternately in a plane parallel to said substrate,

said guard ring pattern including: a groove formed in each of said first and second interlayer insulation films, said groove changing a direction thereof repeatedly and alternatively in a plane parallel to said substrate, a conductive wall [extending] filling said groove in each of said first and second interlayer insulation films and extending from a bottom principal surface thereof to a top principal surface thereof; and a conductive pattern making a contact with a top part of said conductive wall and having a principal surface coincident to said top principal surface of said interlayer insulation film, said conductive wall changing a direction thereof repeatedly and alternately in one of a triangular wave pattern and a rectangular wave pattern in said plane in correspondence to said guard ring pattern,

said conductive wall in said first interlayer insulation film being offset with respect to said conductive wall in said second interlayer insulation film in a direction parallel to a principal surface of said substrate when viewed in a direction perpendicular to said principal surface of said substrate.

6. (Amended) A semiconductor device as claimed in claim 1, wherein said interlayer insulation [film comprises] films comprise a first insulation film that supports said conductive wall laterally and a second insulation film that supports said conductive pattern laterally.